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Interface Control Scheme for Computer High-Speed Interface Unit

An interface control has been developed for a computer high-speed interface unit (HSIU). The control is general and performs for multiplexed and dedicated channels as well as for data-bus interfaces. These are all parts of a space ultrareliable modular computer (SUMC).

The control comprises two 64-pin, dual in-line packages, each of which holds a custom LSI (large-scale integrated) array built with silicon-on-sapphire CMOS (complementary metal-oxide semiconductor) technology. The control, consisting of a control chip and a bus chip, performs all of the following functions:

- a. It receives and amplifies all in tags.
- b. It produces and controls all out tags.
- c. It handles the timing and disbursing of all input and output data and tag sequences.
- d. It performs level conversions between 10-V (HSIU) and 5-V (external) signals.
- e. It detects and processes erroneous inputs and timeouts.
- f. It maintains close communication with the main I/O channel.
- g. It provides holding registers and level conversions for input and output buses.
- h. It checks parity and continuously compares two bus registers.

- i. It provides continuous level conversions for tag lines which go only between the control unit and the central processor.
- j. Finally, it provides its own main and secondary clocks, and operates asynchronously for maximum speed.

Note:

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Patent status:

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